Amendments to the Drawings:

Two new sheets of drawings are provided, having figures 7 and 8 thereon. Figures 7 and 8 show cross-sectional views of the bonding option architectures shown in figurers 4 and 6, respectively. No new matter is added through the new drawings, and acceptance of the new drawings is respectfully requested.

Attachment: New Sheets 2 pages

REMARKS/ARGUMENTS

1. Objection to the specification:

The specification is objected to for describing Figs. 4-5's elements 52 as "lead frames".

The specification is objected to for describing Fig. 6's elements 98 as "lead frames" Correction is required.

Response:

The specification has been amended to change all descriptions of "lead frames" to read "leads". Acceptance of the corrected specification is respectfully requested.

2. Objection to claims 4, 6, and 20:

Response:

Claims 4 and 20 have been amended to change the description of the "lead frames" to read "lead frame". Claim 6 has been cancelled, and is no longer in need of consideration. Acceptance of the amended claims is respectfully requested.

3. Rejection of claims 1, 3-8, 19, and 20 under 35 U.S.C. 112, first paragraph:

Claims 1, 3-8, 19, and 20 are rejected under 35 U.S.C. 112, first paragraph as failing to comply with the enablement requirement. The claimed first and second package substrates are unclear, particularly in the absence of cross-sectional and/or perspective views thereof.

Response:

New sheets of drawings containing figures 7 and 8 have been added to show cross-sectional views of the bonding option architectures shown in figurers 4 and 6, respectively.

The chip packaging structures illustrated in Figures 4 and 6 contain two different package substrates. Each of the package substrates having a different voltage level can be connected to a bonding option pad for allowing the bonding option pad to receive the different voltage levels. Figure 4 shows that a second package substrate 60 surrounds a first package substrate 58 on both the inner and outer sides of the first package substrate 58. Figure 6 shows that a second package substrate 92 surrounds a first package substrate 90 on the outer side of the first package substrate 90. In view of the illustrations in figures 4, 6, 7, and 8, the applicant submits that the claimed first and second package substrates are clearly described in the disclosure, and reconsideration of claims 1, 3-8, 19, and 20 is respectfully requested.

4. Rejection of claims 1, 3-8, 19, and 20 under 35 U.S.C. 102(e):

Claims 1, 3-8, 19, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by McLellan et al. (US 6,995,460, hereinafter McLellan) for reasons of record.

Response:

The applicant would like to point out the patentable differences between independent claim 1 and McLellan. Claim 1 recites that each bonding option pad of the chip is selectively connected to the first package substrate or the second package substrate. As shown in Fig.4, for example, each of the bonding pads 62 can connect to either the first package substrate 58 or the second package substrate 60. Since the first package substrate 58 has a different voltage from the second package substrate 60, the voltage provided to the bonding pad 62 can be determined based on the selected connection to either the first package substrate 58 or the second package substrate 60.

On the other hand, McLellan does not teach that "each bonding option pad of the chip is selectively connected to the first package substrate or the second package substrate", as is recited in claim 1. Instead, McLellan teaches in Figs. 6E-6H that the three bonding wires 205 on each side of the chip 206 are respectively connected to the power/ground ring 204 and the contact pads 203. That is, each of the bonding wires 205 has an assigned connection, and McLellan does not teach that each bonding option pad is selectively connected to either the first package substrate or the second package substrate. Therefore, the voltage level or the signals provided to the bonding option pad cannot be selected in McLellan's design as it can in the claimed structure. For these reasons, the applicant submits that claim 1 is patentably distinct from McLellan, and should be allowable.

Regarding claim 20, McLellan does not teach that each bonding pad of the chip has a corresponding lead, and that each bonding option pad is selectively connected to the first package substrate, the second package substrate, or the corresponding lead. Instead, each bonding pad is assigned to be connected to a contact pad 203 or to the power/ground ring 204. McLellan does not teach that each bonding option pad can be selectively connected to either of first or second package substrates or a corresponding lead. In fact, McLellan's disclosure concerns a "leadless plastic chip carrier" (see title and abstract), and therefore does not teach selectively connecting each bonding pad to a lead at all. For these reasons, claim 20 should also be allowable over McLellan.

Furthermore, claims 3-8, 19, and 20 are all dependent on claim 1, and should be allowed if claim 1 is allowed. Reconsideration of claims 1, 3-8, 19, and 20 is respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)